CLAIMS

What is claimed is:

1. A system comprising a phase shifter circuit, the phase shifter circuit comprising:

an input clock terminal;

an output clock terminal;

an inverter having an input terminal coupled to the input clock terminal and an output terminal;

a first counter circuit having a clock terminal coupled to the input clock terminal and a plurality of output terminals;

a register having a plurality of data input terminals coupled to the output terminals of the first counter circuit, a clock terminal coupled to the input clock terminal, and a plurality of output terminals;

a second counter circuit having a clock start terminal coupled to the input clock terminal, a plurality of clock stop terminals coupled to the output terminals of the register, and an output terminal;

a third counter circuit having a clock start terminal coupled to the output terminal of the inverter, a plurality of clock stop terminals coupled to the output terminals of the register, and an output terminal; and

an output clock generator having a first input terminal coupled to the output terminal of the second counter circuit, a second input terminal coupled to the output terminal of the third counter circuit, and an output terminal coupled to the output clock terminal.

2. The system of Claim 1, wherein the register is one of a divide-by-two register and a divide-by-four register.

3. The system of Claim 1, wherein the phase shifter circuit further comprises a maximum value circuit coupled between the output terminals of the register and the clock stop terminals of the second and third counter circuits.

4. The system of Claim 3, wherein the maximum value circuit comprises:

a plurality of set delay input terminals;

a comparator having a first plurality of input terminals coupled to the set delay input terminals, a second plurality of input terminals coupled to the output terminals of the register, and an output terminal; and

a multiplexer having a first plurality of input terminals coupled to the output terminals of the register, a second plurality of input terminals coupled to the set delay input terminals, a select input terminal coupled to the output terminal of the comparator, and a plurality of output terminals coupled to the clock stop terminals of the second and third counter circuits.

5. The system of Claim 1, further comprising an adder circuit coupled between the first counter circuit and the register.

6. The system of Claim 1, further comprising a decrementer circuit coupled between the first counter circuit and the register.

7. The system of Claim 1, wherein the first counter circuit comprises:

a first oscillator circuit having an input terminal coupled to the input clock terminal and further having an output terminal; and

a first counter having an input terminal coupled to the output terminal of the first oscillator circuit and further having a plurality of output terminals coupled to the data input terminals of the first register.

8. The system of Claim 7, wherein the second and third counter circuits each comprise:

a second oscillator circuit having an input terminal coupled to the input clock terminal and further having an output terminal, the second oscillator circuit being implemented to oscillate with the same frequency as the first oscillator circuit;

a second counter having an input terminal coupled to the output terminal of the second oscillator circuit and further having a plurality of output terminals; and

a comparator having a first set of input terminals coupled to the output terminals of the register, a second set of input terminals coupled to the output terminals of the second counter, and an output terminal coupled to a corresponding one of the first and second input terminals of the output clock generator.

9. The system of Claim 1, wherein the phase shifter circuit further comprises a reset input terminal coupled to reset input terminals of the first counter circuit, the register, the second counter circuit, and the third counter circuit.

10. The system of Claim 1, wherein the output clock generator comprises a set input terminal coupled to the output terminal of the second counter circuit, a reset input terminal coupled to the output terminal of the third counter circuit, and an output terminal coupled to the output clock terminal.

11. The system of Claim 10, wherein the output clock generator comprises a flip-flop having a data input terminal coupled to power high VDD, a clock terminal coupled to the output terminal of the second counter circuit, a reset terminal coupled to the output terminal of the third counter circuit, and an output terminal coupled to the output clock terminal.

12. The system of Claim 1, wherein the first counter circuit comprises means for resetting itself after each M input clock periods, wherein M is an integer.

13. The system of Claim 12, wherein M is five.

14. The system of Claim 1, wherein the system comprises a programmable logic device (PLD), and the phase shifter circuit is implemented using programmable logic of the PLD.

15. The system of Claim 14, wherein the PLD is one of a field programmable gate array (FPGA) and a complex programmable logic device (CPLD).

16. A system comprising a phase shifter circuit, the phase shifter circuit comprising:

an input clock terminal;

an output clock terminal;

a first counter circuit having a clock terminal coupled to the input clock terminal and a plurality of output terminals;

a first register having a plurality of data input terminals coupled to the output terminals of the first counter circuit, a clock terminal coupled to the input clock terminal, and a plurality of output terminals;

a second counter circuit having a clock start terminal coupled to the input clock terminal, a plurality of clock stop terminals coupled to the output terminals of the first register, and an output terminal;

a third counter circuit having a clock start terminal coupled to the output terminal of the second counter circuit, a plurality of clock stop terminals coupled to the output terminals of the first counter circuit, and an output terminal; and

an output clock generator having a first input terminal coupled to the output terminal of the second counter circuit, a second input terminal coupled to the output terminal of the third counter circuit, and an output terminal coupled to the output clock terminal.

17. The system of Claim 16, wherein the first register is one of a divide-by-two register and a divide-by-four register.

18. The system of Claim 16, wherein the clock stop terminals of the third counter circuit are coupled to the output terminals of the first counter circuit via the first register.

19. The system of Claim 16, wherein the phase shifter circuit further comprises a second register, and wherein the clock stop terminals of the third counter circuit are coupled to the output terminals of the first counter circuit via the second register.

20. The system of Claim 19, wherein the second register is a divide-by-two register.

21. The system of Claim 16, wherein the phase shifter circuit further comprises a maximum value circuit coupled between the output terminals of the first register and the clock stop terminals of the second counter circuit.

22. The system of Claim 21, wherein the maximum value circuit comprises:

a plurality of set delay input terminals;

a comparator having a first plurality of input terminals coupled to the set delay input terminals, a second plurality of input terminals coupled to the output terminals of the first register, and an output terminal; and

a multiplexer having a first plurality of input terminals coupled to the output terminals of the first register, a second plurality of input terminals coupled to the set delay input terminals, a select input terminal coupled to the output terminal of the comparator, and a plurality of output terminals coupled to the clock stop terminal of the second counter circuit.

23. The system of Claim 16, further comprising an adder circuit coupled between the first counter circuit and the first register.

24. The system of Claim 16, further comprising a decrementer circuit coupled between the first counter circuit and the first register.

25. The system of Claim 16, further comprising a duty cycle correction (DCC) enable circuit coupled between the output terminal of the second counter circuit and the clock start terminal of the third counter circuit, and further coupled between the output terminals of the first counter circuit and the clock stop terminals of the third counter circuit.

26. The system of Claim 16, wherein the first counter circuit comprises:

a first oscillator circuit having an input terminal coupled to the input clock terminal and further having an output terminal; and

a first counter having an input terminal coupled to the output terminal of the first oscillator circuit and further having a plurality of output terminals coupled to the data input terminals of the first register.

27. The system of Claim 26, wherein the second and third counter circuits each comprise:

a second oscillator circuit having an input terminal coupled to the input clock terminal and further having an output terminal, the second oscillator circuit being implemented to oscillate with the same frequency as the first oscillator circuit;

a second counter having an input terminal coupled to the output terminal of the second oscillator circuit and further having a plurality of output terminals; and

a comparator having a first set of input terminals coupled to the output terminals of the first register, a second set of input terminals coupled to the output terminals of the second counter, and an output terminal coupled to a corresponding one of the first and second input terminals of the output clock generator.

28. The system of Claim 16, wherein the phase shifter circuit further comprises a reset input terminal coupled to reset input terminals of the first counter circuit, the first register, the second counter circuit, and the third counter circuit.

29. The system of Claim 16, wherein the output clock generator comprises a set input terminal coupled to the output terminal of the second counter circuit, a reset input terminal coupled to the output terminal of the third counter circuit, and an output terminal coupled to the output clock terminal.

30. The system of Claim 29, wherein the output clock generator comprises a flip-flop having a data input terminal coupled to power high VDD, a clock terminal coupled to the output terminal of the second counter circuit, a reset terminal coupled to the output terminal of the third counter circuit, and an output terminal coupled to the output clock terminal.

31. The system of Claim 16, wherein the first counter circuit comprises means for resetting itself after each M input clock periods, wherein M is an integer.

32. The system of Claim 31, wherein M is five.

33. The system of Claim 16, wherein the system comprises a programmable logic device (PLD), and the phase shifter circuit is implemented using programmable logic of the PLD.

34. The system of Claim 33, wherein the PLD is one of a field programmable gate array (FPGA) and a complex programmable logic device (CPLD).

35. A method of providing a phased output clock signal from an input clock signal, the method comprising:

counting a first number of counts between two successive initial edges of the input clock signal;

determining a delay value based at least in part on the first number;

counting a second number of counts following each initial edge of the input clock signal and comparing the second number with the delay value;

providing a first edge on the output clock signal when the second number reaches the delay value;

counting a third number of counts following each following edge of the input clock signal and comparing the third number with the delay value; and

providing a second edge on the output clock signal when the third number reaches the delay value.

36. The method of Claim 35, wherein determining a delay value based at least in part on the first number comprises:

determining a maximum value based at least in part on the first number;

comparing a set delay with the maximum value;

selecting the set delay as the delay value if the set delay does not exceed the maximum value; and

selecting the maximum value as the delay value if the set delay exceeds the maximum value.

37. The method of Claim 36, wherein determining a maximum value based at least in part on the first number comprises dividing the first number by two to obtain the maximum value.

38. The method of Claim 36, wherein determining a maximum value based at least in part on the first number comprises dividing the first number by four to obtain the maximum value.

39. The method of Claim 36, wherein determining a maximum value based at least in part on the first number comprises adding together one-half of the first number and one-quarter of the first number to obtain the maximum value.

40. The method of Claim 36, wherein determining a maximum value based at least in part on the first number comprises subtracting a predetermined value from the first number to obtain the maximum value.

41. The method of Claim 35, wherein counting a first number of counts between two successive initial edges of the input clock signal is repeated every M periods of the input clock signal, wherein M is an integer.

42. The method of Claim 41, wherein M is five.

43. The method of Claim 35, wherein the steps of the method are performed by a circuit implemented in a programmable logic device (PLD).

44. The method of Claim 43, wherein the PLD is one of a field programmable gate array (FPGA) and a complex programmable logic device (CPLD).

45. The method of Claim 35, wherein the first edges and the initial edges are both rising edges, and the second edges and the following edges are both falling edges.

46. A method of providing a phased output clock signal from an input clock signal, the method comprising:

counting a first number of counts between two successive initial edges of the input clock signal;

determining a duty cycle correction (DCC) value based at least in part on the first number;

determining a delay value;

counting a second number of counts following each initial edge of the input clock signal and comparing the second number with the delay value;

providing a first edge on the output clock signal when the second number reaches the delay value;

counting a third number of counts following each first edge on the output clock signal and comparing the third number with the DCC value; and

providing a second edge on the output clock signal when the third number reaches the DCC value.

47. The method of Claim 46, wherein determining a DCC value based at least in part on the first number comprises dividing the first number by one of two and four to obtain the DCC value.

48. The method of Claim 46, wherein determining a delay value comprises:

determining a maximum value;

comparing a set delay with the maximum value;

selecting the set delay as the delay value if the set delay does not exceed the maximum value; and

selecting the maximum value as the delay value if the set delay exceeds the maximum value.

49. The method of Claim 48, wherein determining a maximum value comprises dividing the first number by two to obtain the maximum value.

50. The method of Claim 48, wherein determining a maximum value comprises dividing the first number by four to obtain the maximum value.

51. The method of Claim 48, wherein determining a maximum value comprises adding together one-half of the first number and one-quarter of the first number to obtain the maximum value.

52. The method of Claim 48, wherein determining a maximum value comprises subtracting a predetermined value from the first number to obtain the maximum value.

53. The method of Claim 46, wherein counting a first number of counts between two successive initial edges of the input clock signal is repeated every M periods of the input clock signal, wherein M is an integer.

54. The method of Claim 53, wherein M is five.

55. The method of Claim 46, wherein the steps of the method are performed by a circuit implemented in a programmable logic device (PLD).

56. The method of Claim 55, wherein the PLD is one of a field programmable gate array (FPGA) and a complex programmable logic device (CPLD).

57. The method of Claim 46, wherein the first edges and the initial edges are both rising edges, and the second edges and the following edges are both falling edges.